CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Original) A method comprising:

receiving an input clock signal having a first set of edges and a second set of edges;

receiving a first set of data values associated with the first set of edges of the input clock signal and a second set of data values associated with the second set of edges of the input clock signal;

providing a first clock signal with a first clock manager in response to the input clock signal, wherein the first clock signal has a third set of edges that are synchronous with the first set of edges of the input clock signal;

storing the first set of data values in response to the third set of edges of the first clock signal;

providing a second clock signal with a second clock manager in response to the input clock signal, wherein the second clock signal has a fourth set of edges that are synchronous with the second set of edges of the input clock signal; and

storing the second set of data values in response to the fourth set of edges of the second clock signal.

2. (Original) The method of Claim 1, wherein the first set of edges of the input clock signal are rising edges of the input clock signal, and wherein the second set of edges of the input clock signal are falling edges of the input clock signal.

3. (Original) The method of Claim 1, wherein the step of providing the second clock signal in response to the input clock signal comprises inverting the input clock signal.

4. (Original) The method of Claim 3, wherein the step of providing the second clock signal in response to the input clock signal further comprises comparing the second clock signal with the inverted input clock signal.

5. (Original) The method of Claim 1, wherein the step of providing the first clock signal in response to the input clock signal comprises comparing the first clock signal with the input clock signal.

6. (Original) The method of Claim 1, wherein the input clock signal has an asymmetric duty cycle.

7. (Original) The method of Claim 6, wherein the first and second clock signals have substantially a 50-50 duty cycle.

8. (Original) The method of Claim 1, wherein the first set of data values are even data words of a data stream and the second set of data values are odd data words of the data stream.

9. (Original) The method of Claim 1, further comprising:

adjusting the third set of edges of the first clock signal such that the third set of edges occur substantially at a center of a first data window associated with the first set of data values; and

adjusting the fourth set of edges of the second clock signal such that the second set of edges occur substantially at a center of a second data window associated with the second set of data values.

10. (Original) A clock management system comprising:

a clock input terminal configured to receive an input clock signal having a first set of edges and second set of edges;

a data input terminal configured to receive a first set of data values associated with the first set of edges of the input clock signal and a second set of data values associated with the second set of edges of the input clock signal;

a first clock manager coupled to the clock input terminal and configured to provide a first clock signal on a first clock terminal in response to the input clock signal, wherein the first clock signal has a third set of edges that are synchronous with the first set of edges of the input clock signal;

a first register coupled to the first clock terminal and the data input terminal, wherein the first register is configured to latch the first set of data values in response to the third set of edges of the first clock signal;

a second clock manager coupled to the clock input terminal and configured to provide a second clock signal on a second clock terminal in response to the input clock signal, wherein the second clock signal has a fourth set of edges that are synchronous with the second set of edges of the input clock signal; and

a second register coupled to the second clock terminal and the data input terminal, wherein the second register is configured to latch the second set of data values in response to the fourth set of edges of the second clock signal.

11. (Original) The clock management system of Claim 10, wherein the first set of edges of the input clock signal are rising edges of the input clock signal, and wherein the second set of edges of the input clock signal are falling edges of the input clock signal.

12. (Original) The clock management system of Claim 10, wherein the input clock signal has an asymmetric duty cycle.

13. (Original) The clock management system of Claim 12, wherein the first and second clock signals have substantially a 50-50 duty cycle.

14. (Original) The clock management system of Claim 10, further comprising an inverter coupled between the clock input terminal and the second clock manager.

15. (Original) The clock management system of Claim 10, wherein the first clock manager and the second clock manager each comprise at least one of a phase locked loop and a delay locked loop.

16. (Original) The clock management system of Claim 10, wherein the first set of data values are even data words of a data stream and the second set of data values are odd data words of the data stream.

17. (Original) The clock management system of Claim 10, further comprising:

a first phase adjustment block coupled to the first clock manager to adjust the third set of edges of the first clock signal such that the third set of edges occur substantially at a center of a first data window associated with the first set of data values; and

a second phase adjustment block coupled to the second clock manager to adjust the fourth set of edges of the second clock signal such that the second set of edges occur substantially at a center of a second data window associated with the second set of data values.

18. (Original) A clock management system comprising:

means for receiving an input clock signal having a first set of edges and a second set of edges;

means for receiving a first set of data values associated with the first set of edges of the input clock signal and a second set of data values associated with the second set of edges of the input clock signal;

means for providing a first clock signal in response to the input clock signal, wherein the first clock signal has a third set of edges that are synchronous with the first set of edges of the input clock signal;

means for storing the first set of data values in response to the third set of edges of the first clock signal;

means for providing a second clock signal in response to the input clock signal, wherein the second clock signal has a fourth set of edges that are synchronous with the second set of edges of the input clock signal; and

means for storing the second set of data values in response to the fourth set of edges of the second clock signal.

19. (Original) The clock management system of claim 18, wherein the first set of edges of the input clock signal are rising edges of the input clock signal, and wherein the second set of edges of the input clock signal are falling edges of the input clock signal.

20. (Original) The clock management system of Claim 18, further comprising means for inverting the input clock signal.

21. (Original) The clock management system of Claim 18, wherein the input clock signal has an asymmetric duty cycle.

22. (Original) The clock management system of Claim 18, further comprising:

means for adjusting the third set of edges of the first clock signal such that the third set of edges occur substantially at a center of a first data window associated with the first set of data values; and

means for adjusting the fourth set of edges of the second clock signal such that the second set of edges occur substantially at a center of a second data window associated with the second set of data values.